MBI5030 Application Note

Foreword

MBI5030 is specifically designed for LED video applications using *internal* Pulse Width Modulation (PWM) control, unlike the traditional LED drivers with *external* PWM control, with selectable 16-bit or 12-bit color depth, providing outstanding grayscale performance.

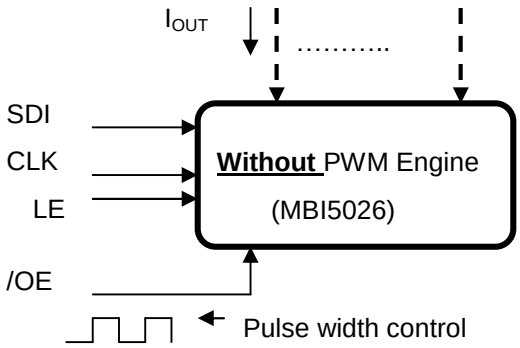

Fig. 1. The traditional LED driver

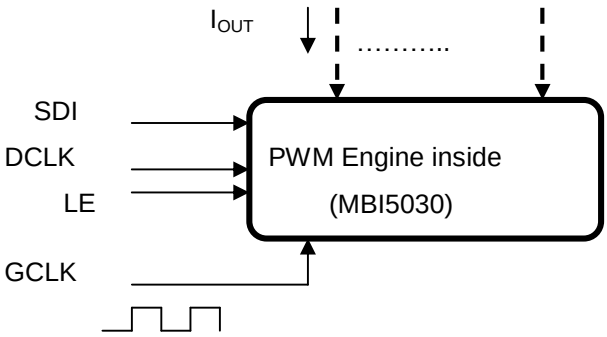

Fig. 2. PWM-Embedded LED driver

Figure 1 shows the schema of the traditional LED driver. The traditional LED driver adjusts LED current (I_{OUT}) or LED brightness by sending different pulse width PWM signals through /OE pin. However, the signal at /OE pin will result in the signal distortion and the signal decay due to a long distance transmission. The phenomenon causes a poor brightness control for LED while using more grayscale bits.

Figure 2 shows the schema of PWM-embedded LED driver. The PWM-embedded LED driver adjusts LED current (I_{OUT}) or LED brightness by triggering the internal PWM engine through GCLK. Similarly, the signal at GCLK pin will result in the signal distortion and the signal decay due to a long distance transmission, but the signal distortion and the signal decay of GCLK do not affect brightness control for LED while using more grayscale bits. Since GCLK is just a triggered clock, its pulse width can be ignored for the operations of PWM-Embedded engine.

The operations between MBI5030 (PWM-Embedded) and MBI5026 are quite different in several aspects, such as the input method of the image data and the settings of the grayscale. Detailed operations are described in the following sections.

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1. Principle of Operations

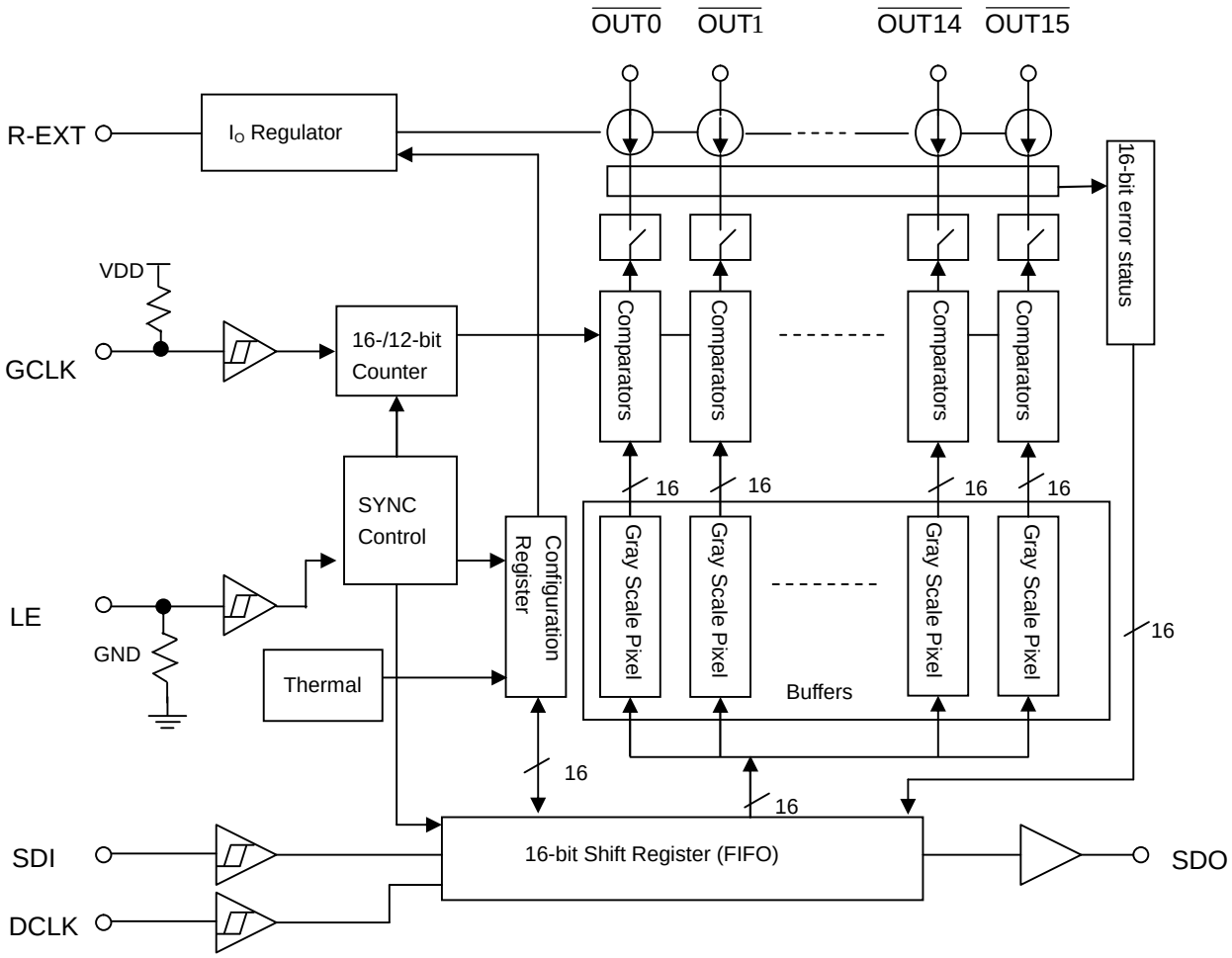

Fig. 3. MBI5030 Block Diagram

Figure 3 presents the block diagram of MBI5030. The function of each pin is described below:

1. Input pins of control signals

DCLK: Data Clock Input pin. DCLK samples the signal of SDI and LE on its rising edge.

SDI: Grayscale Data Input pin. Serial data input with DCLK.

LE: Controlling command with DCLK.

The grayscale data can be transmitted to MBI5030 at the right timing with the signals of DCLK, SDI and LE. MBI5030 reads one bit datum of SDI into the internal 16-bit shift register on the rising edge of DCLK. The signal of LE handles the data-latch of the internal 16-bit shift register.

2. Output pin of control signals

SDO: Serial Data Output pin. The first device of SDO is connected to the second device of SDI, i.e., transmitting grayscale data to the next MBI5030.

3. Input pin of PWM counter clock

GCLK: PWM Counter Clock Input pin. The frequency of GCLK determines the count speed to the internal PWM counter, i.e., PWM frequency on every /OUT0 ~ /OUT15.

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4. Setting pin of output current

R-EXT: Rext is used to connect an external resistor to set up output current for all output channels.

5. Output Pins of constant current

/OUT0~/OUT15: I_{OUT} output channel pin. Generally, every channel can connect one or more LEDs depending on the circuit design.

2. The basic setting of grayscale

Sixteen output channels of MBI5030 can receive different grayscale data individually.

The data length of the grayscale setting of each channel is 16 bits, so the data length of 16 channels is total 256 bits (16 bits x 16 channels = 256 bits). Therefore, a complete data length of each MBI5030 is 256 bits. Note: No matter PWM grayscale counter is either 16 bits or 12 bits, a complete data length is still 256 bits. This is a constraint of the IC internal circuit. Detailed descriptions are as below.

Regarding the delivering method of grayscale data, to set one channel output current requires one set data (16 bits). That means to set 16 channels output current requires 16 sets data (256 bits) in the MBI5030. The sequence of delivering data is from OUT15 firstly then OUT14 …, and till OUT0.

The 16-bit shift register latches 15 times of grayscale data into each data buffer with a data-latch command sequentially. With a global-latch command for the 16th grayscale data, the 256-bit data buffers will be clocked in with the MSB first, loading the data from channel 15 to channel 0.

Bit 15 to bit 12 of the grayscale data of one channel are invalid in a 12-bit grayscale counter mode, but the 4 bits are still required to be transmitted by 4 zeros to the device. This is because that the shift register of MBI5030 is 16 bits so that the second MBI5030 can receive exactly the same 16 bits grayscale data via the first MBI5030. The table 2-1 lists which bits should fill with zero for MBI5030 and MBI5030 while using 12-bit PWM. Especially, bit3 ~bit0 should fill with zero while MBI5030 sets to 16-bit PWM counter mode and it uses 12-bit grayscale.

Table 2-1 The data zero-padding of MBI5030/31 while using 12-bit PWM

Device	MBI5030	MBI5030	MBI5031
PWM counter	16-bit	12-bit	12-bit
Zero-padding	Bit 3 ~ Bit 0	Bit 15 ~ Bit 12	Bit 15 ~ Bit 12

The function of each data-latch is that grayscale data of 16 bits are latched into 16-bit shift register, but the buffer of every channel are not updated on the fly. The data-latch has to repeat 15 times. However, a global-latch is used for the 16th data-latch. It also updates the contents of the buffer of every channel on the fly.

As for when the grayscale data of every channel will be updated to 16 output channels, it depends on the mode setting in the configuration register. Refer to section 6 for more details.

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3. The setting of grayscale data when cascading MBI5030

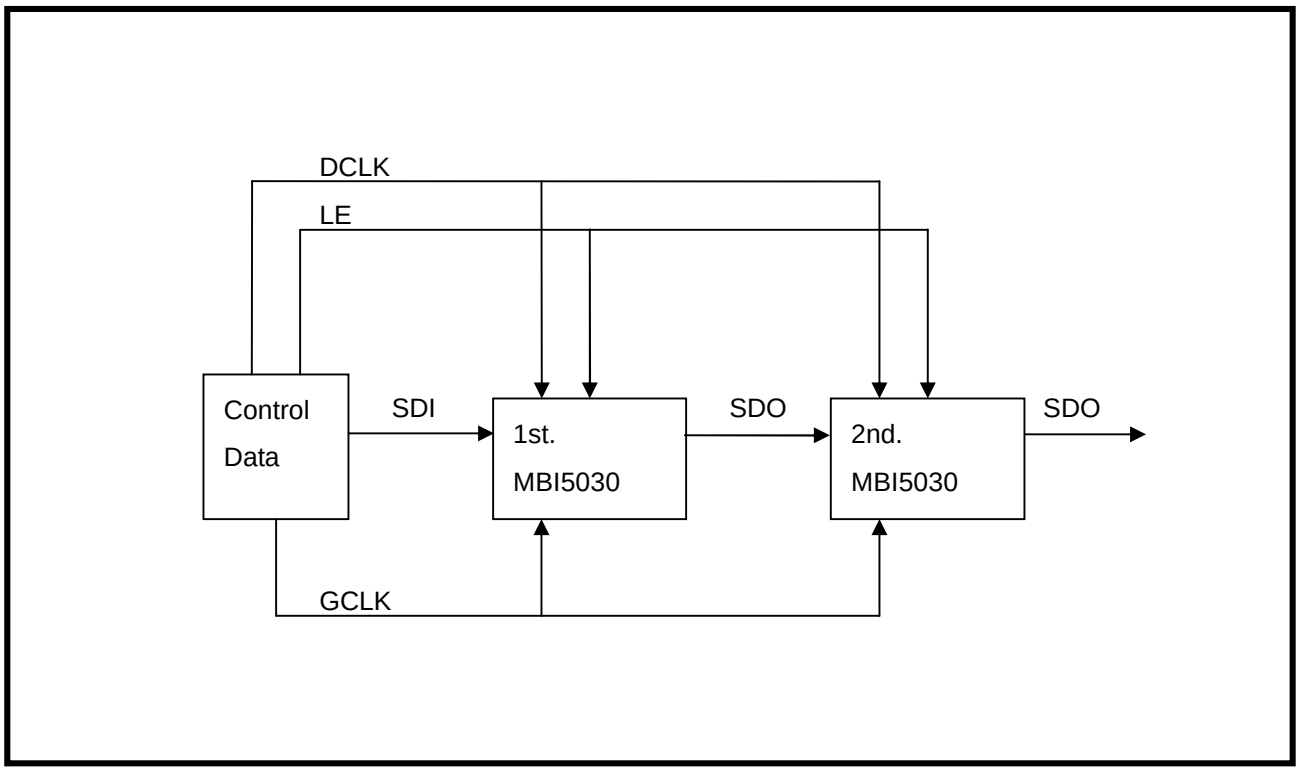

Fig. 4. Cascade of two MBI5030s

Figure 4 shows the cascade of two MBI5030s. If users cascade N pieces of MBI5030s, 16 x N bits data will be transmitted on every latch signal.

One latch signal latches grayscale data of 16 bits for one MBI5030.

One latch signal latches grayscale data of 32 bits for the cascade of two MBI5030s.

One latch signal latches grayscale data of 48 bits for the cascade of three MBI5030s.

The latch signal can not latch the correct data until all of the grayscale data are all set as Figure 5 and Figure 6.

See the datasheet on page 10 about the introduction of the control commands of MBI5030/MBI5031.

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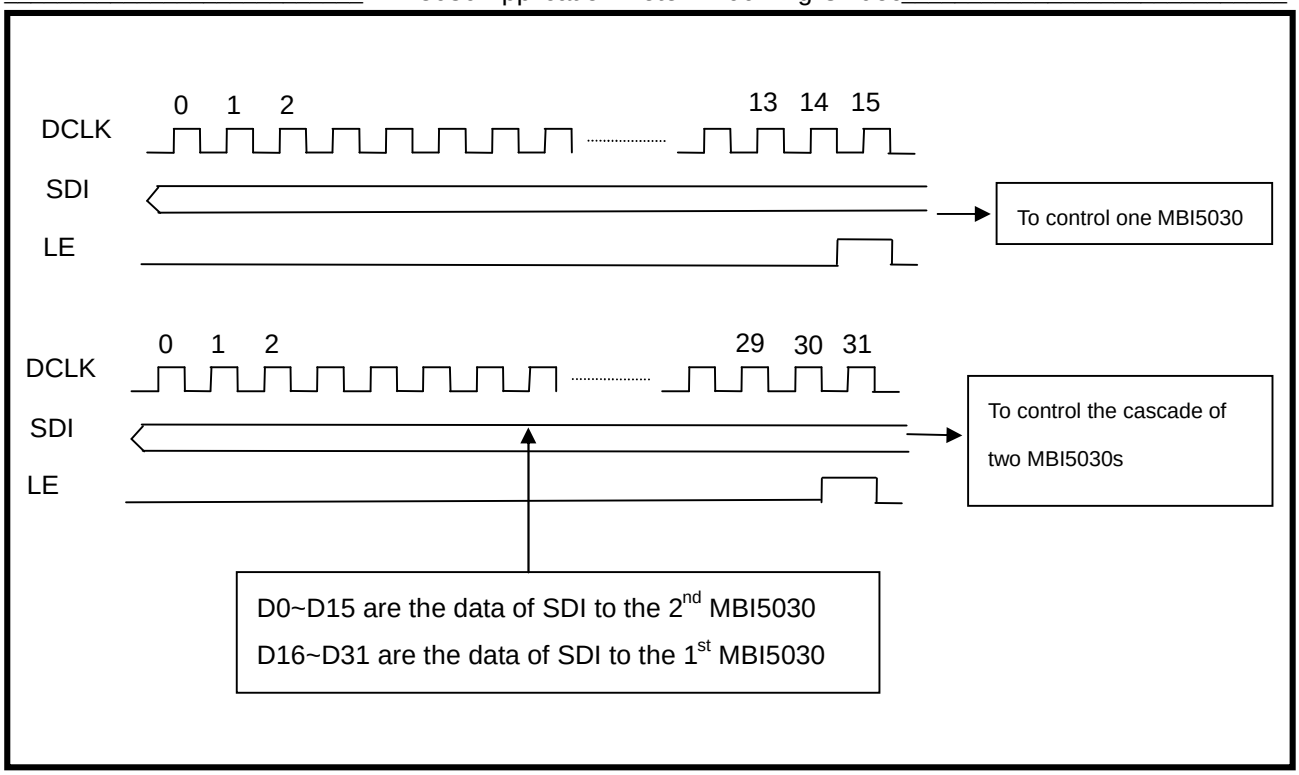

Fig. 5. The timing diagram of data-latch

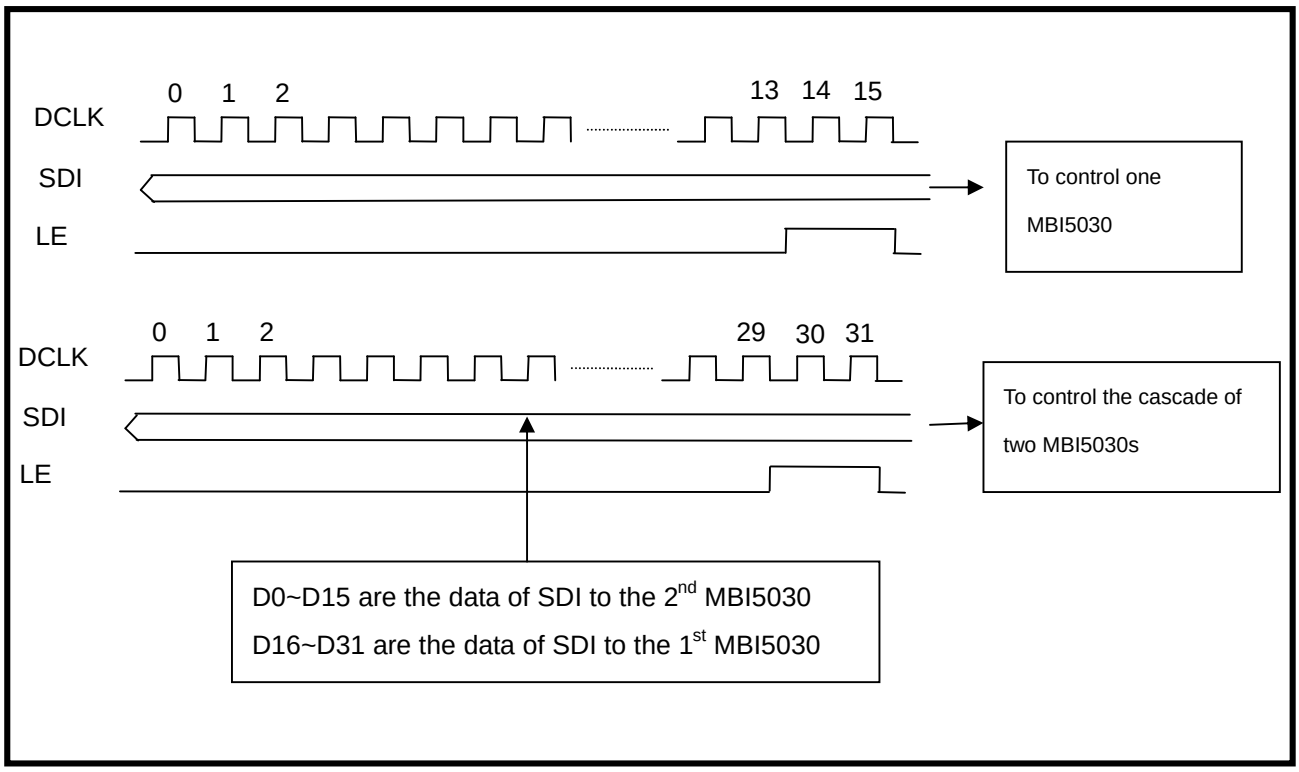

Fig. 6. The timing diagram of global-latch

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4. Read/Write Configuration Register

The readable and writable configuration register of MBI5030 can determine the operation mode. The configuration register controls the settings of PWM grayscale counter, PWM count mode selection, PWM data synchronization mode, the adjustment of current gain and time-out alert.

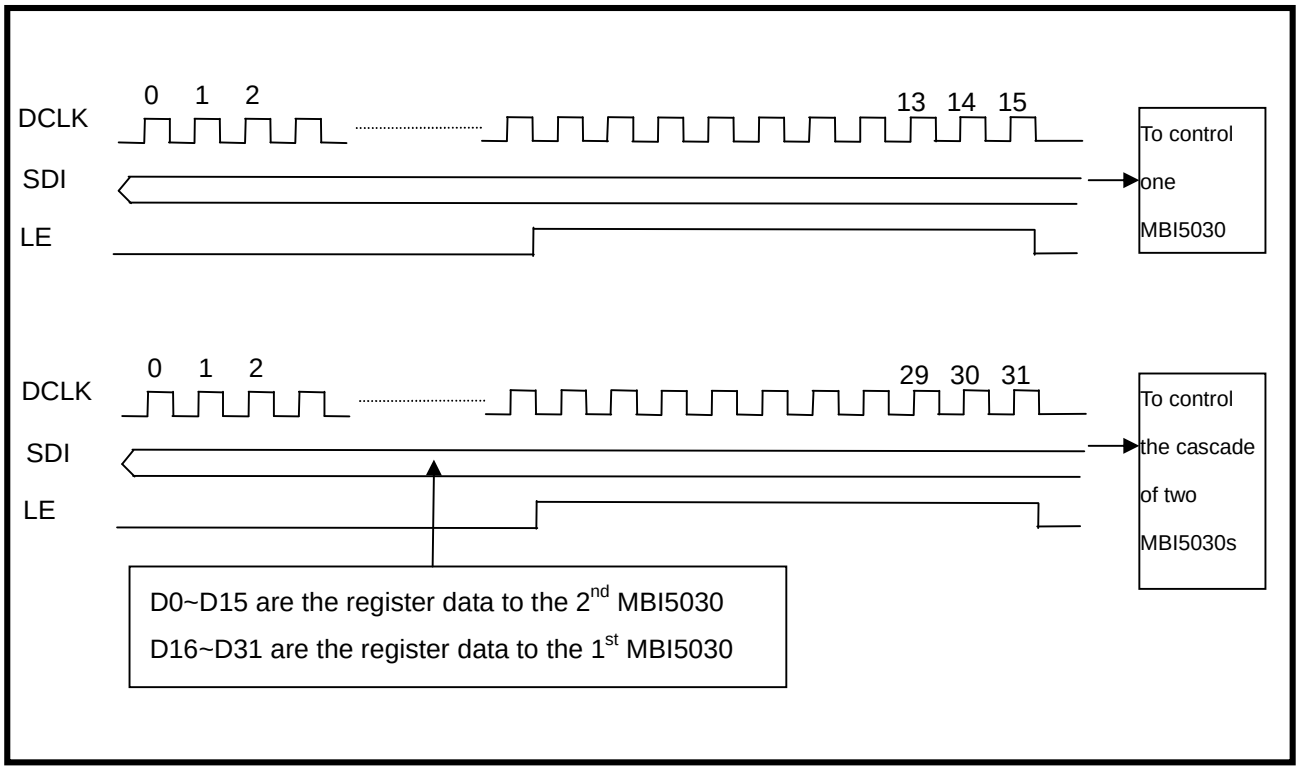

Fig. 7. The timing diagram of “Write Configuration”

Figure 7 illustrates how to set the operation mode of “write configuration”.

The method of controlling the command of “write configuration” is similar to that of controlling data-latch and global-latch. See section 3 for more details. Similarly, a latch signal latches 16-bit data for one MBI5030. A latch signal latches 32-bit data for the cascade of two MBI5030s.

Therefore, data 0~15 of configuration register write to the 2nd MBI5030 and data 16 ~ 31 of configuration register write to the 1st MBI5030 while two MBI5030s are cascaded. Feeding data to SDI starts with MSB first. Note: all of MBI5030 commands are triggered on the falling edge of LE.

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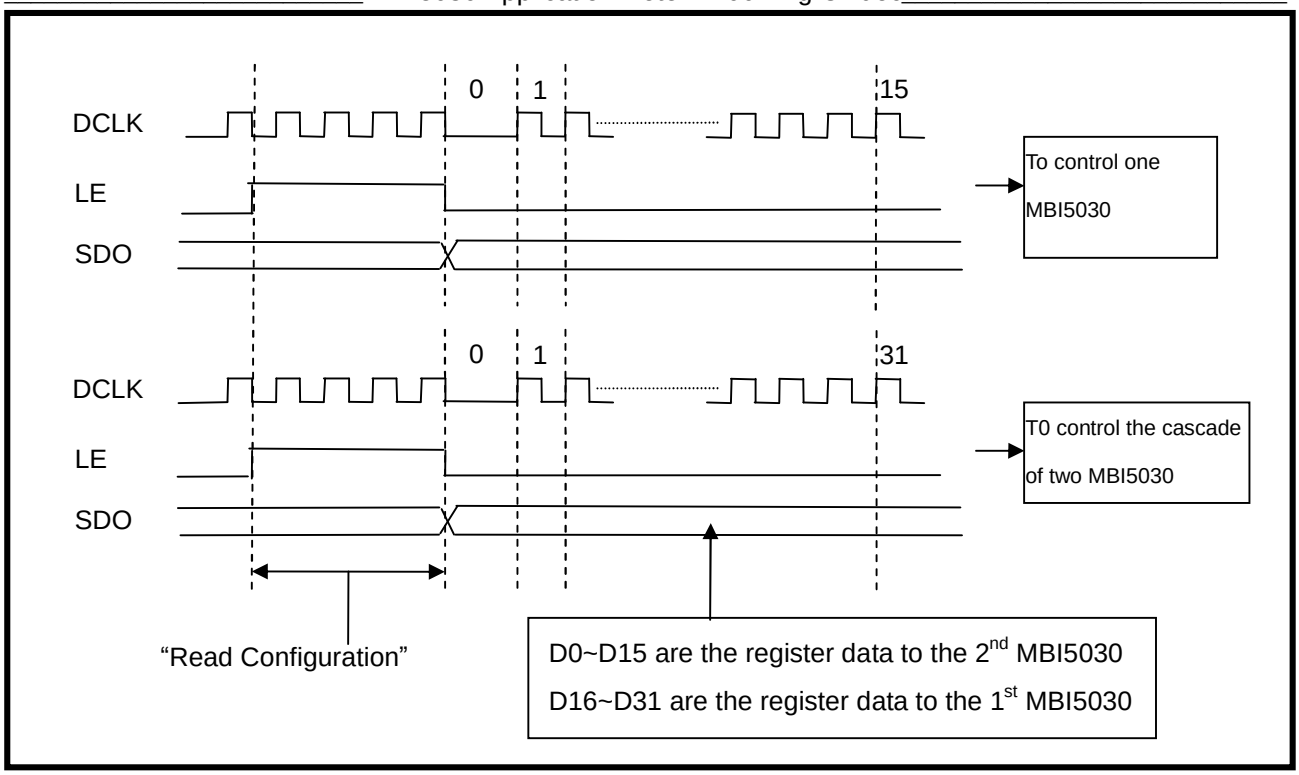

Fig. 8. The timing waveform of "Read-Configuration"

Figure 8 illustrates how to read the contents of the configuration register. MBI5030 reads the contents of the configuration register into SDO when the high pulse width of LE contains 4 or 5 rising edges of DCLK.

SDO will have a response (bit F) immediately on the falling edge of LE. Next, bit E to bit 0 of the configuration register will be read out successively on the rising edge of DCLK. In other words, the bit sequence of the configuration register can be read out from bit F (MSB) to bit 0 (LSB) in order. The signal of SDI can be ignored during "Read Configuration".

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5. The constraints of MBI5030 applied in multiplexing type of LED display board

MBI5030 can be applied in multiplexing type operation in LED display board. Because MBI5030 needs 256 bits data to fill up 16 channels in one MBI5030, users need to calculate the data frame rate carefully. Otherwise, an insufficient data frame rate will affect the image performance in LED display. The detailed description is shown in the following sections.

Figure 9 shows the schematic of multiplexing type operation in LED display. Figure 10 shows the static type operation in LED display.

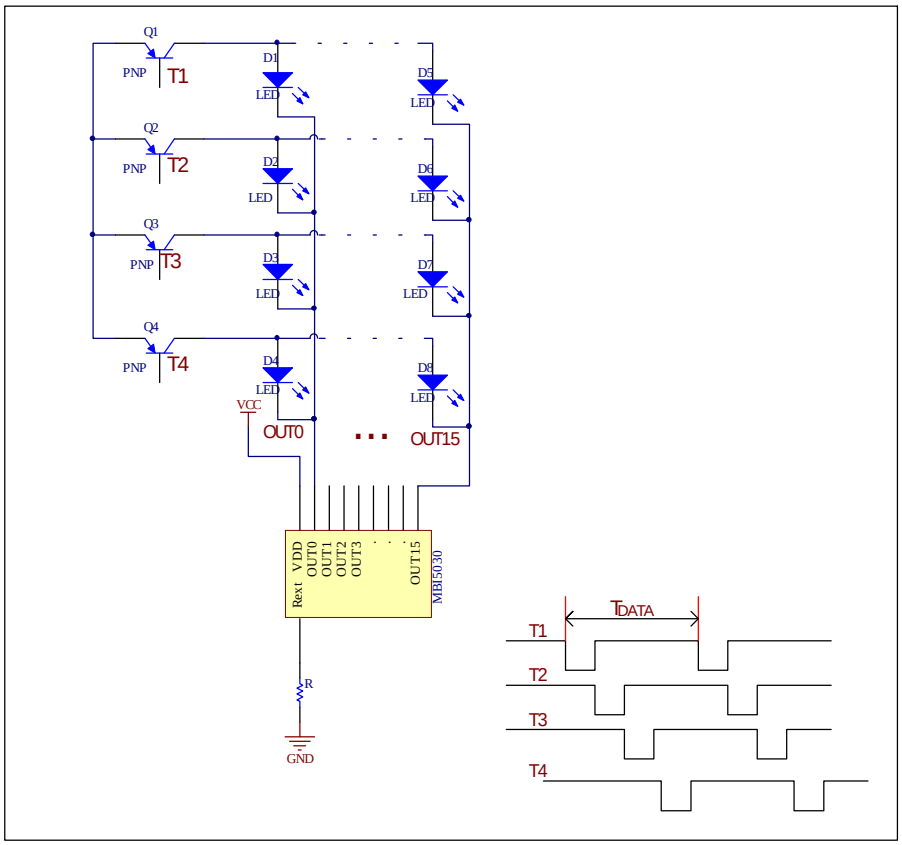

Fig. 9. Schematic of multiplexing type LED board with MBI5030

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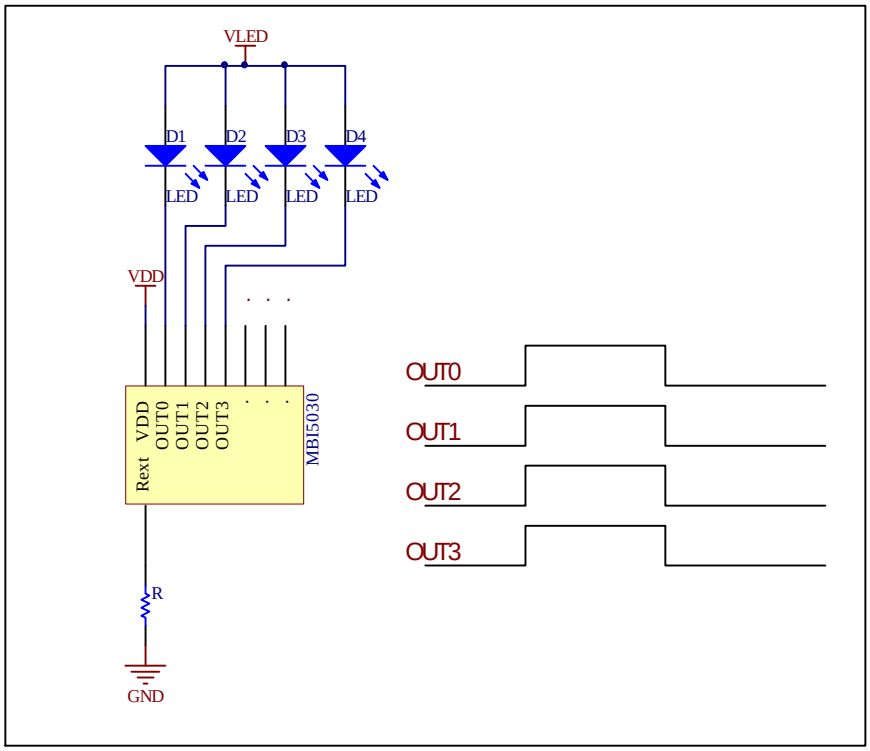

Fig. 10. Schematic of static-type LED board with MBI5030

Users need to consider the following 2 issues when employing MBI5030 in the multiplexing type application since MBI5030 is built with PWM grayscale counter.

1. The speed of PWM grayscale counter needs to follow the speed of data frame rate.

That means PWM grayscale counter must complete one cycle counting before all data are loaded in MBI5030s. Otherwise, every channel of MBI5030 will not have a completed PWM duty cycle. Therefore, the design must conform to the following equation:

$$F_{GCLK} / 2^{Grayscale} / F_{DATA} \geq 1,$$

where

F_{GCLK}: GCLK frequency

F_{DATA}: Data frame rate

Grayscale: grayscale bits (16 bits or 12 bits)

T_{DATA}: the period of data update (=1/F_{DATA}), refer to Fig. 9.

For example, given 16-bit grayscale counter, data refresh rate 60Hz/second, and GCLK frequency 8MHz,

$(8 \times 10^6)/2^{16}/60=2.03$,

The calculation result is 2, means that the data will take twice PWM cycles. Therefore, at most 1/2 duty of time multiplexing can be reached in such condition.

In the condition of 16-bit grayscale counter, it will take more time to finish one cycle counting. Therefore, the

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16-bit grayscale counter is not suitable for multiplexing type application.

Given 12-bit grayscale counter, data refresh rate 60Hz/second, and GCLK frequency 8MHz,

$(8x10^6)/2^{12}/60=32.55$,

The calculation result is 32, means that the data will take 32 times of PWM cycles. Therefore, at most 1/32 duty of time multiplexing can be reached in the above condition.

The frequency of GCLK is an important factor in time multiplexing type application.

Table 5-1 The duty cycle number at GCLK=8MHz in time multiplexing application

Case	Bit numbers of grayscale control	Frame rate (Hz)	Cycle numbers of GCLK counter in a period T_{DATA}	Duty cycle of multiplexing design
1	16 bit	60	2	1/2 duty
2	12 bit	60	32	1/32 duty
3	16 bit	30	4	1/4 duty
4	12 bit	30	64	1/64 duty

2. Make sure the time of T_{DATA} is enough to update all of data for MBI5030s.

The volume of grayscale data transmission is huge for PWM driver IC. Take MBI5030 for example, one MBI5030 needs 256 bits. When MBI5030s are employed in time multiplexing type application referring to Figure 9, the data refresh rate needs to be concerned because the switches (T1~T4) have fast switching speed. Otherwise, the grayscale counter will be probably interrupted by the next turned on switch (T1~T4). The number of cascaded MBI5030 is also an important factor to affect data refresh rate. The equation of calculating the maximum cascade numbers is shown as below.

$$N = (F_{DCLK} \times Duty)/(256 \times F_{DATA}),$$

where

N: the maximum cascade numbers

F_{DCLK}: frequency of serial data

F_{DATA}: Data frame rate

Duty: duty cycle for one LED

The more numbers of LEDs are in every channel, the shorter time it takes in one LED in time multiplexing application and the fewer cascaded MBI5030s are needed. Take case 4 in table 5-2 for example, the frame rate is 60Hz/sec and the frequency of DCLK is 25MHz with 1/8 duty cycle. The calculation result of the cascade number of MBI5030 is:

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N = [(25x10^6) x (1/8)]/(256 x 60)=203.

The frequency of DCLK and the duty time on one LED are the two main factors to affect the maximum cascade numbers of MBI5030.

Table 5-2 The maximum cascade numbers of MBI5030 at DCLK=25MHz

Case	Frame rate (Hz)	Duty cycle of multiplexing design	Turned on time of every LED	The maximum cascade numbers of MBI5030
1	60	1 duty	16.66ms	1627
2	60	1/2 duty	8.33ms	813
3	60	1/4 duty	4.165ms	406
4	60	1/8 duty	2.082ms	203
5	60	1/16 duty	1.041ms	101
6	30	1 duty	33.33ms	*3255*
7	30	1/2 duty	16.66ms	*1627*
8	30	1/4 duty	8.33ms	*813*
9	30	1/8 duty	4.165ms	*406*
10	*30*	*1/16 duty*	*2.082ms*	*203*

To have a complete grayscale control in the display system, the above 2 issues have to be conformable when applying the MBI5030 in the time multiplexing application.

6. The differences between auto-synchronization mode and manual-synchronization mode

The bit definition of the configuration register is as follows:

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Bit A of the configuration register means selecting PWM data synchronization mode, auto-synchronization or manual-synchronization. Auto-synchronization mode is suitable for static type LED display, and manual-synchronization mode is suitable for time multiplexing type LED display.

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When the MBI5030 operates in auto-synchronization mode, grayscale data loaded by the terminal of signal control will store in the internal buffer of MBI5030 till PWM counter counts the new period of MSB PWM then update the grayscale data. The advantage of auto-synchronization mode is that the signal control side does not need to care about the synchronization issue between display image and grayscale data update. In auto-synchronization mode, MBI5030 only needs a GCLK with fixed frequency and then MBI5030 can automatically update data in the correct timing. At the moment, the grayscale counter will not be interrupted by the next new grayscale data. Besides, the speed of PWM counter has to be faster than the speed of data refresh. A relationship between F_{GCLK} and F_{DATA} is shown as following.

$$F_{GCLK} / 2^{Grayscale} / F_{DATA} > 1,$$

Where

F_{GCLK}: frequency of GCLK

F_{DATA}: Data frame rate

Grayscale: the depth of grayscale (16 bits or 12 bits)

Although auto-synchronization mode has some advantages, it is only suitable for static type LED display. Manual-synchronization mode is suitable for time multiplexing type because the turned-on duty cycle of every LED has to be controlled in time multiplexing type LED display.

7. LED Open-Circuit Detection

Open-circuit detection of MBI5030 has two processes, “Enable Error Detection” and “Read Error Status Code”. ”Enable Error Detection” executes the detection and stores the results of the detection in the 16-bit error status register of MBI5030. ”Read Error Status Code” reads the contents of the 16-bit error status register into SDO pin.

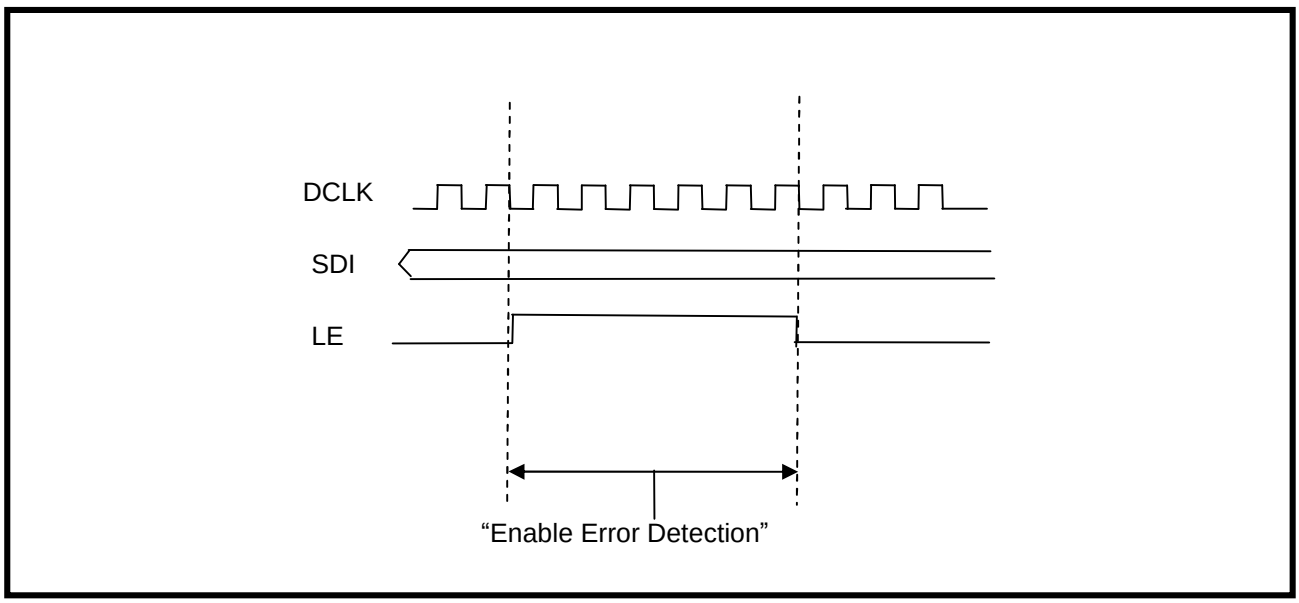

Fig. 13. The timing diagram of “Enable Error Detection”

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The timing diagram of “Enable Error Detection” is as Figure 13. MBI5030 executes the operation of Open-Circuit Detection when the high pulse width of LE contains 6 or 7 rising edges of DCLK.

The signals of SDI can be ignored while the command of “Enable Error Detection” is operating.

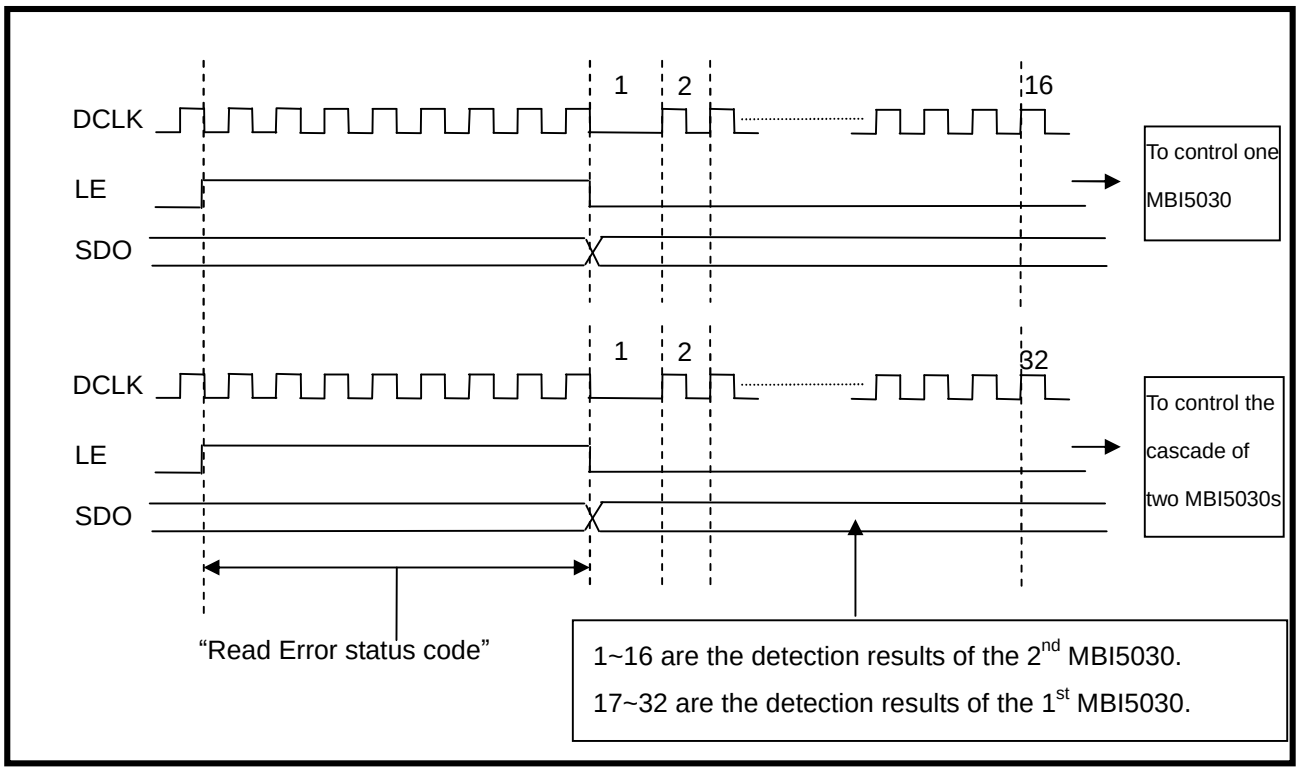

Fig. 14. The timing diagram of “Read Error Status Code”

The timing diagram of “Read Error Status Code” is as Figure 14. The error status of open-circuit detection is 16 bits for one MBI5030, because each MBI5030 has 16 output channels. The detection results of open-circuit detection will be loaded into the internal 16-bit shift register of MBI5030 when the high pulse width of LE contains 8 or 9 rising edges of DCLK.

SDO will have a response immediately on the falling edge of LE. Next, the remaining data with 15 bits will be read out successively on the rising edge of DCLK, so the data sequence at SDO pin is the detection results of OUT15, OUT14,…, OUT0 in order.

After understanding the above commands, users also need to pay attention to the following issues when operating the open-circuit detection:

1. The command, “Enable Error Detection” will enforce all output channels to be turned on for open-circuit detection when MBI5030 receives the command. No matter what previous status is, all output channels are asserted. All output channels restore the previous status after MBI5030 receives “Read Error Status Code”. At least 1us is required to obtain the stable error status resulted from “Read Error Status Code”.
2. The device will quit the mode of “Error Detection” and restore the previous status of 16 output channels automatically when the device does not receive “Read Error Status Code” over 1ms after “Enable Error Detection” is activated.

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3. The error detection principle of MBI5030 is shown as Fig. 15.

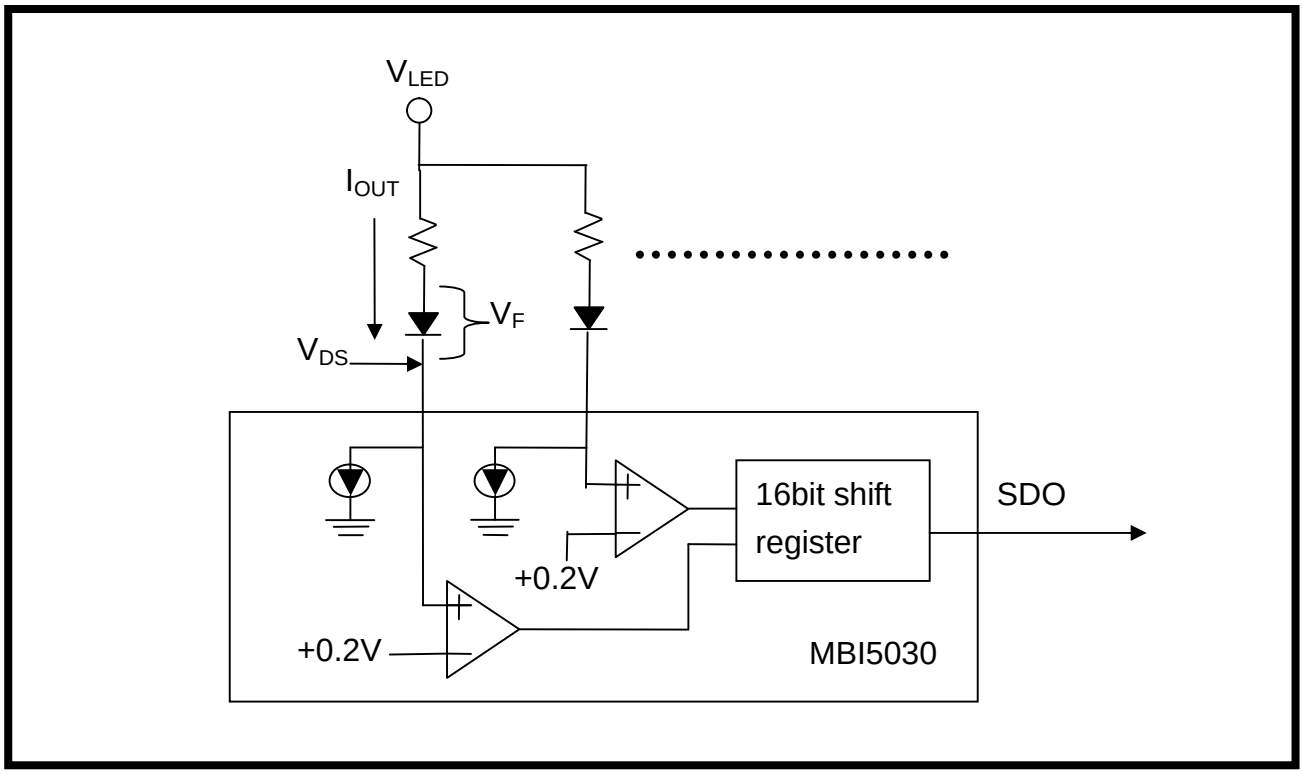

Fig. 15. The function block of MBI5030 error detection

I_{OUT}: output current

V_F: LED forward voltage

V_{DS}: output pins voltage

The principle of error detection is to make a comparison between VDS and 0.2V, and then shift the detection results through SDO pin.

4. Please make sure that V_{DS} (the voltage of every output channel) is greater than 0.5V while every output channel is turned on for open-circuit detection.
   When LEDs are broken or opened, the corresponding test results will show value '1' because V_{DS} voltage, 0V, is smaller than 0.2V.
   When LEDs are normal, the corresponding test results will show value '0' because V_{DS} voltage, 0.5V, is greater than 0.2V.
5. Please make sure that V_{DS} (the voltage of every output channel) is less than 0.2V while every output channel is turned on for short-circuit detection. The test result '0' means that LEDs are broken with short circuit and '1' means that LEDs work normally. The required voltage of V_{DS} can be achieved through adjusting V_{LED}.
6. The voltage (V_{DS}) of output channels should be avoided between 0.2V and 0.5V, because such voltage range can not work normally either in Open-Circuit Detection mode or in Short-Circuit Detection mode. Table 7-1 shows the error detection conditions.

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Table 7-1 Error detection conditions

LED error detection	Recommended V_{DS}	LED status	Compare results	Test results code
LED Open detection	Above 0.5V	open	V_{DS} < 0.2V	“1”
		normal	V_{DS} > 0.2V	“0”
LED Short detection	Under 0.2V	normal	V_{DS} < 0.2V	“1”
		short	V_{DS} > 0.2V	“0”
Undetermined region	Between 0.2V and 0.5V	Please avoid the V_{DS} range		

8. Time-Out Alert

MBI5030 also has Time-Out Alert function. The function is used to prevent output channels from getting an abnormal output current when GCLK stops by accident.

To monitor GCLK so that no matter GCLK is stuck at zero or stuck at one, the data stored in the device will be cleared and MBI5030 will turn off 16 output channels after 1 second. Therefore, to resume GCLK start counting, the grayscale data have to be resent in order to enable 16 output channels of MBI5030.

For example, the LED current in time multiplexing LED display application will be several times larger than that in static type LED display application for the same LED brightness. Therefore, large current will probably pass through LEDs when GCLK stops by accident because the driver output will keep the “on” status when GCLK stops by accident, if the Time-Out Alert function is disabled. If the Time-Out Alert function is enabled, there will be no issue of LED inrush current when GCLK stops by accident in time multiplexing LED display application.

Users can enable or disable the function of Time-Out Alert by setting the Configuration Register.

9. Suggestions

1. The frequency of GCLK is limited to 25MHz. The condition is under the resolution of 16 bits grayscale. A higher frequency of GCLK can be applied when grayscale resolution is less than 16 bits. This is good for LED’s demonstration.

2. The system design of MBI5030s can adopt the distributed SDI input (SDI_0~SDI_n) on many MBI5030s instead of the cascade of MBI5030 for the high volume data transmission.

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